

Dhaka International University

Lab Report details:

**Lab Report Topic**: Implementation and Verification of a Logic Circuit Using Basic Gates  
**Lab Report No** :02  
**Course Title** : Digital Logic Design Lab  
**Course Code** :

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# Experiment Title:

Implementation and Verification of a Logic Circuit Using Basic Gates

# Objective:

To design, implement, and verify the logic function F = (AB + CD)' using basic logic gates (AND, OR, and NOT).

# Components Required:

- Logic trainer kit or simulation software (e.g., Multisim/Proteus/Logisim)  
- Logic gates: AND, OR, NOT  
- Connecting wires  
- Power supply

# Theory:

The given Boolean expression is: F = (AB + CD)'  
  
This is a NAND of two AND operations:  
1. First, AND gates are used to perform the operations AB and CD.  
2. The outputs of the AND gates are then input to an OR gate: AB + CD.  
3. The output of the OR gate is then passed through a NOT gate to give the final output F.  
  
Thus, the circuit implements the NAND operation of two ANDed terms.

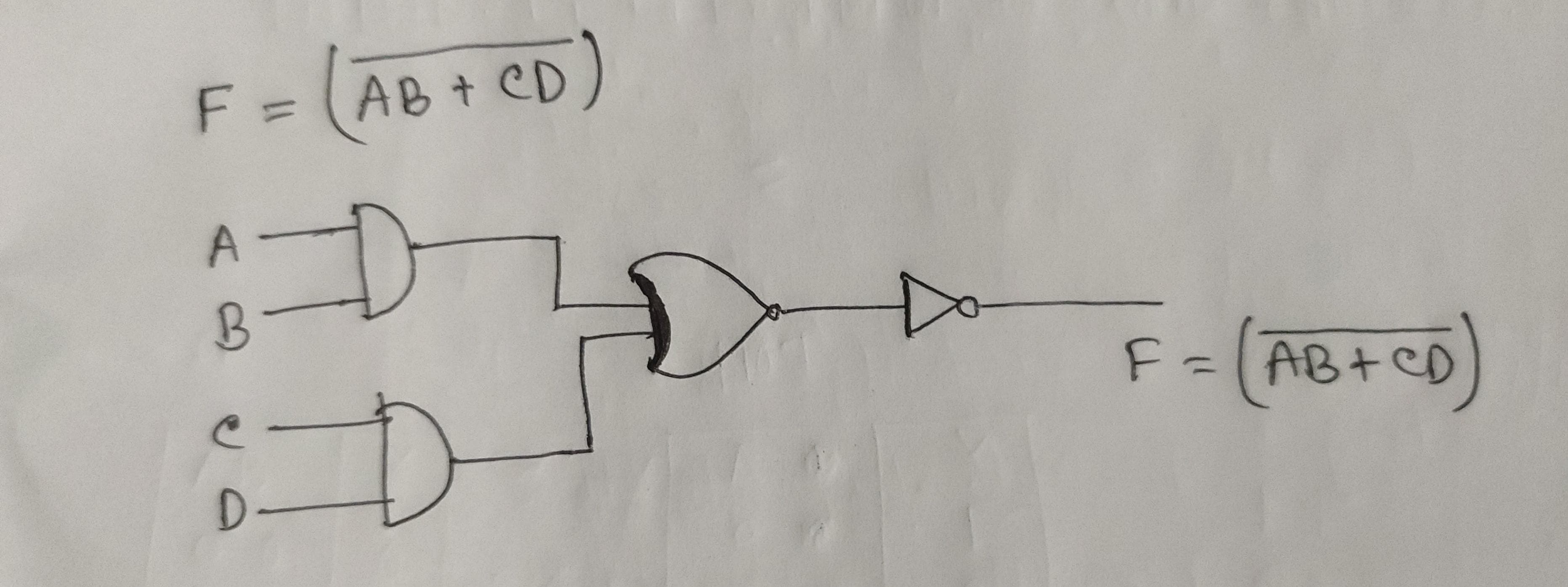
# Procedure:

1. Connect inputs A, B, C, and D to logic switches.  
2. Connect A and B to the first AND gate, and C and D to the second AND gate.  
3. Connect the outputs of both AND gates to the inputs of the OR gate.  
4. Connect the output of the OR gate to the input of a NOT gate.  
5. Connect the output of the NOT gate to the output LED or logic probe to observe the result.  
6. Vary the input combinations and observe the corresponding output.

# Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F = (AB + CD)' |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |

# Circuit Diagram:



# Observation:

The output F is HIGH (1) only when both AB and CD are not simultaneously high; otherwise, it is LOW (0), as per the NAND logic behavior.

# Conclusion:

The circuit successfully implements the Boolean function F = (AB + CD)' using basic gates. The output matches the expected results for all input combinations, verifying the correctness of the design.